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HO, TU TU V

ART UNIT	PAPER NUMBER
2818	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/943,134	Applicant(s) FORBES ET AL.	
	Examiner Tu-Tu Ho	Art Unit 2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 October 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-84* is/are pending in the application.

4a) Of the above claim(s) *24-84* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/ Restriction

1. Applicant's election without traverse of claims 1-23, directed to a vertical channel floating gate transistor, in Paper No. 8 filed 04 November 2002 is acknowledged with appreciation. However, claims 1-23 are directed to both a vertical channel floating gate (FG) transistor and a planar channel FG transistor; and upon close examination of the claims, so far as device claims are concerned as in the case of claims 1-23, vertical channel FG transistor and planar channel FG transistor are only obvious design choices. Accordingly, claims 1-23 are examined and claims 24-84 are withdrawn from consideration in this office action.

Specification

2. Applicant is reminded to update the information and/or status of the co-pending applications disclosed in the specifications.

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections/ Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter that the applicant regards as his invention.

4. Claims 14-17 and 23 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

- Claim 14 recites "The vertical non volatile memory cell" which lacks an antecedent basis. As best as can be understood, claim 14 is dependent on claim 10.

- Claim 15 recites "The vertical floating gate" which lacks an antecedent basis. As best as can be understood, claim 15 is dependent on claim 14.

- Claim 16 recites "The vertical non volatile memory cell" which lacks an antecedent basis. As best as can be understood, claim 16 is dependent on claim 10.

- Claim 17 recites "The vertical non volatile memory cell" and "the horizontally oriented floating gate" which lack an antecedent basis. As best as can be understood, claim 17 is dependent on claim 16.

- Claim 23 is not proper because it does not refer back to all limitations of a previous claim. See MPEP § 608.01(n). As best as can be understood, claim 23 is dependent on claim 18 (assuming that a device having a first and second source/drain regions and a floating gate is a floating gate transistor).

5. Claims 2 and 10 are objected to because of the following informalities/typographical errors:

- These claims recite:

"wherein the aluminum oxide has a number of small compositional ranges such that gradients which produce different barrier heights at an interface with the floating gate and control gate" which appears to be incomplete. Perhaps the phrase should be:

"wherein the aluminum oxide has a number of small compositional ranges such that gradients can be formed by an applied electric field which produce different barrier heights at an interface with the floating gate and control gate".

6. Claims 8 and 13 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim, Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Specifically, these claims recite: "the low tunnel barrier intergate insulator" instead of "the asymmetrical low tunnel barrier intergate insulator" thus failing to further limit the subject matter.

Normally, theses problems are not critical; however, in the instant case, as applicants are aware, there is a co-pending application (SN 09/945507) having 80 claims that are essentially similar to the claims of the present invention if one were to disregard the limitation "asymmetrical".

Appropriate correction is required.

Double Patenting

7. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed.

Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

8. Claims 1-23 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1-23 of copending Application No. 10/081,818 and over claim 1-22 of copending Application No. 10/028,001. Although the conflicting claims are not identical, they are not patentably distinct from each other.

Referring to claims 1, 10, and 18, claims 1, 10, and 18 of Application No. 10/081,818 recite a semiconductor memory device as claimed but fail to disclose that the claimed floating gate (FG) transistor is a depletion mode FG transistor. However, not only that depletion mode FG transistor and enhancement mode FG transistor involves only design parameters, the limitation "depletion mode" appears only in the preamble and would be considered non-limitation.

Regarding claim 9, although claim 1 of Application No. 10/028,001 recites a p-channel FG transistor as opposed to an n-channel FG transistor, one of ordinary skill in the art would recognize that n-channel and p-channel transistors involve only dopants and materials used.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in

(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or

(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The figures and reference numbers referred to in this Office Action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

9. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Faraone U.S. Patent 4,757,360.

Faraone discloses in Figures 1-6 and respective portions of the specification a floating gate transistor, comprising:

a first source/drain region and a second source/drain region separated by a channel region in a substrate;

a floating gate 20 opposing the channel region and separated therefrom by a gate oxide 18;

a control gate 30 opposing the floating gate; and

wherein the control gate is separated from the floating gate by an asymmetrical low tunnel barrier intergate insulator 26 (having a textured surface, hence asymmetrical, as being termed by Faraone).

10. Claim 10 is rejected under 35 U.S.C. §103(a) as being unpatentable over Faraone U.S. Patent 4,757,360.

Faraone discloses a FG transistor as claimed but fails to disclose a body region. However, as indicated above in paragraph 1 about design choices of planar and vertical FG transistors, it would have been obvious to one of ordinary skill in the art at the time the invention

was made to modify the Faraone's structure to include a body region to make it a vertical FG transistor.

11. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by and claim 10 under 35 U.S.C. §103(a) as being unpatentable over Uchida U.S. Patent 6,229,175.

Similarly as in paragraphs 9 and 10 above, Uchida discloses in Figures 18-22, particularly Figure 18, and respective portions of the specification a device as claimed. Specifically, Uchida discloses a floating gate transistor, comprising:

a first source/drain region 12 and a second source/drain region 11 separated by a channel region (no designation) in a substrate 10;

a floating gate 14 opposing the channel region and separated therefrom by a gate oxide 13;

a control gate 16 opposing the floating gate; and

wherein the control gate is separated from the floating gate by an asymmetrical low tunnel barrier intergate insulator 15 (having a "low barrier height" (Abstract), having two columns 500 and 510 having different barrier heights, each column comprising alternate layers of silicon oxide or silicon nitride and semiconductor or metal having different barrier heights – hence, asymmetrical).

12. Claims 1-6, 9-11, and 14-17 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Lee et al. U.S. Patent 5,923,056 (patent '056).

Patent '056 discloses in Figures 2-4 and respective portions of the specification a doped, metal oxide dielectric material for use as an intergate insulator between a floating gate and a control gate (second embodiment, column 4, lines 36+), wherein the metal oxide is a Group III or Group VB metal oxide (e.g. Al.sub.2 O.sub.3, Y.sub.2 O.sub.3, Ta.sub.2 O.sub.5 or V.sub.2 O.sub.5) and the metal dopant is a Group IV material (Zr, Si, Ti, and Hf), and wherein the metal oxide contains about 0.1 weight percent to about 30 weight percent of the dopant (Abstract). Although Patent '056 does not label the aluminum oxide layer 124 being "an asymmetrical low tunnel barrier intergate insulator" (ALTBII) as claimed by Applicant, Fig. 2 of patent '056 does not distinguish from the claimed structure. Further, the labels nonetheless are meaningless. The patent '056's structure anticipates Applicant's claimed structure regardless of whether the layer is labeled "asymmetrical low tunnel barrier". See *In re Pearson* , 181 USPQ 642; Fx parte Minks 169 USPQ 120; or *In re* Swinehart 169 USPQ 226, all of which make it clear that mere "labels" or "statements of intended use" as we have here in "asymmetrical low tunnel barrier intergate insulator" do not distinguish over patent '056's structure which may be likewise labeled.

With respect to the limitation "wherein the aluminum-oxide-containing asymmetrical low tunnel barrier intergate insulator having a number of small compositional ranges such that gradients can be formed by an applied electric field which produce different barrier heights at an interface with the floating gate and control gate", it would appear that the doped metal oxide layer 124, to be doped with about 0.1 weight percent to about 30 weight percent of the dopant which would be non-uniform to some extent, which would appear to exhibit a number of small

compositional ranges such that gradients can be formed by an applied electric field which produce different barrier heights at an interface with the floating gate and control gate.

13. Claims 1-23 are rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Nguyen et al. U.S. Patent Application No. 2002/0137250.

Nguyen et al. disclose in Figure 6 and respective portions of the specification a high k dielectric film to be used as an intergate insulator layer 58 (paragraph [0036]), wherein the intergate insulator layer 58 is graded (hence, asymmetrical) with among the lanthanum, nitrogen, or aluminum (Abstract). As noted above in paragraph 12 about "statement of intended use", although Nguyen does not term layer 58 an ALTBII as claimed by Applicant, layer 58 contains Al_xO_y and is graded, therefore, it would appear that layer 58 is asymmetrical and exhibits a number of small compositional ranges such that gradients can be formed by an applied electric field which produce different barrier heights at an interface with the floating gate and control gate.

With respect to claims 7, 8, 12, 13, 18, and 19, it would have been obvious to one of ordinary skill in the art at the time the invention was made to select metal as barrier layers 56 and 58.

14. Claims 1-23 are rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Lee et al. U.S. Patent Application No. 2002/0106536 (Application '536).

Application '536 discloses a multi-layer dielectric layer structure for use as an intergate insulator 14/15, wherein the intergate insulator layer 14/15 comprises a silicate interface layer 12 and alternate layers 18 and 20 of HfO.sub.2 or ZrO.sub.2 layers and an Al.sub.2O.sub.3 layer. Although Application '536 does not term the intergate insulator layer 14 an asymmetrical low tunnel barrier intergate insulator, it probably would have been easier to prove that layer 14, comprising alternate layers 18 and 20 of different materials, asymmetrical and exhibiting a number of small compositional ranges such that gradients can be formed by an applied electric field which produce different barrier heights at an interface with the floating gate and control gate, than it is to prove that the claimed aluminum oxide layer 215 of the present invention an asymmetrical low tunnel barrier intergate insulator. And, it probably would have been easier to prove that layers 12 or 18 (referring to claims 7, 12, and 18, the floating gate includes a polysilicon floating gate having a metal layer 12 or 18 formed thereon in contact with the asymmetrical low tunnel barrier intergate insulator 18/20 or 20/18) and top layer 20 (referring to claims 8, 13, and 19, the control gate includes a polysilicon control gate having a metal layer 20 formed thereon in contact with the low tunnel barrier intergate insulator 20/18"), being formed of different materials, having different work functions, than it is to prove that metal layer 216 and 217, whose materials are not disclosed anywhere in the instant application, having different work functions.

Conclusion

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (703) 305-0086. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (703) 308-4910. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Tu-Tu Ho
December 30, 2002

HOAI HO
PRIMARY EXAMINER